



# P-Channel 80-V (D-S) MOSFET

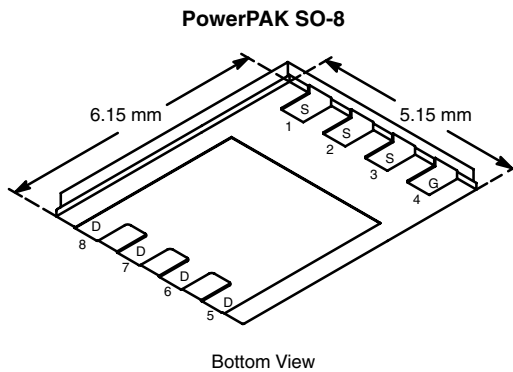
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ)
- 80	0.025 at V <sub>GS</sub> = - 10 V	- 28	55 nC
	0.029 at V <sub>GS</sub> = - 4.5 V	- 28	

## FEATURES

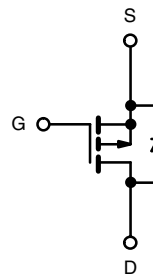
- TrenchFET<sup>®</sup> Power MOSFET



RoHS  
COMPLIANT



Ordering Information: Si7469DP-T1-E3 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 80	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 28 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	- 28 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	- 10.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	- 8.1 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	- 40		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	- 28 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	- 4.3 <sup>b, c</sup>	
Avalanche Current	I <sub>AS</sub>	- 45		
Single-Pulse Avalanche Energy	E <sub>AS</sub>	100	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	83	W
		T <sub>C</sub> = 70 °C	53	
		T <sub>A</sub> = 25 °C	5.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	19	24	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	1.2	1.5	

Notes:

- a. Package Limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 sec.
- d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 65 °C/W.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 80			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 79.6		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	- 40			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -10.2\text{ A}$		0.021	0.025	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -8.1\text{ A}$		0.024	0.029	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -10.2\text{ A}$		52		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4700		pF
Output Capacitance	$C_{oss}$			320		
Reverse Transfer Capacitance	$C_{rss}$			235		
Total Gate Charge	$Q_g$	$V_{DS} = -40\text{ V}, V_{GS} = -10\text{ V}, I_D = -10.2\text{ A}$		105	160	nC
		$V_{DS} = -40\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10.2\text{ A}$		55	85	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -40\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10.2\text{ A}$		16		
Gate-Drain Charge	$Q_{gd}$			26		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		4		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 4.9\text{ }\Omega$ $I_D \cong -8.1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		45	70	ns
Rise Time	$t_r$			220	330	
Turn-Off Delay Time	$t_{d(off)}$			95	145	
Fall Time	$t_f$			110	165	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 4.9\text{ }\Omega$ $I_D \cong -8.1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	$t_r$			25	40	
Turn-Off Delay Time	$t_{d(off)}$			105	160	
Fall Time	$t_f$			100	150	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			- 28	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				- 40	
Body Diode Voltage	$V_{SD}$	$I_S = -8.1\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -8.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		55	85	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			110	165	nC
Reverse Recovery Fall Time	$t_a$			37		ns
Reverse Recovery Rise Time	$t_b$			18		

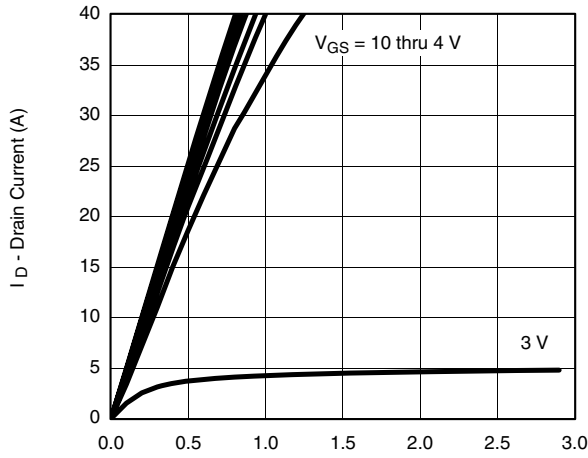
## Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

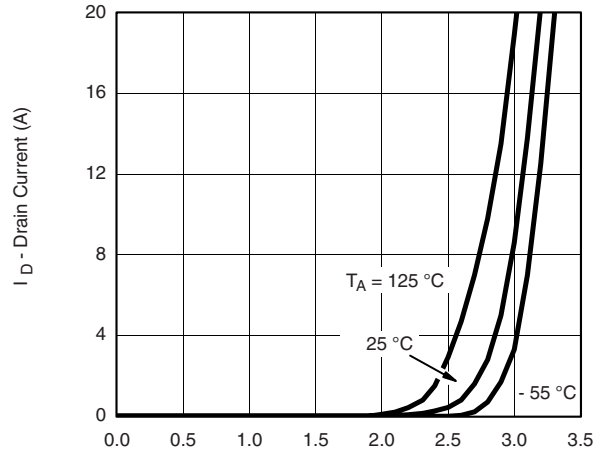
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



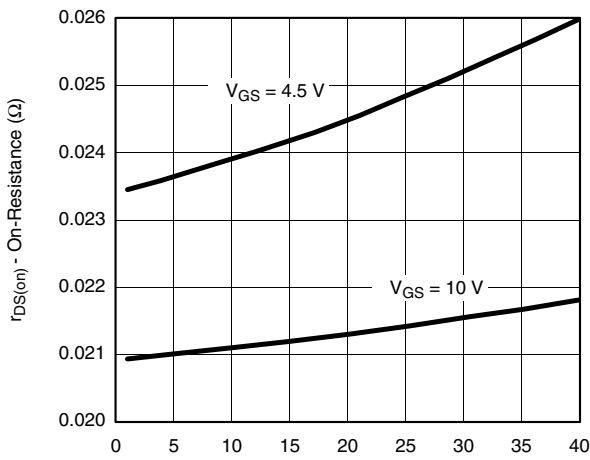
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



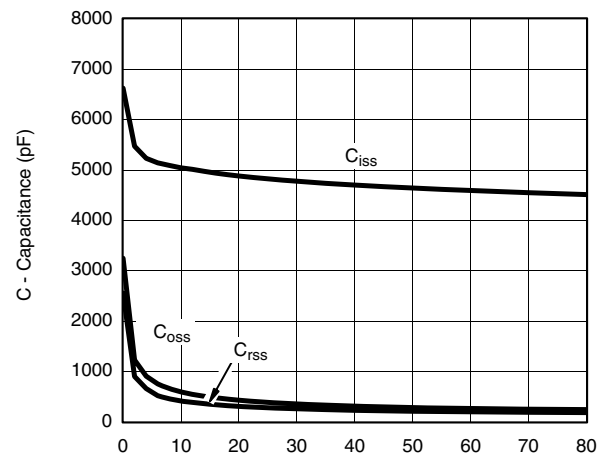
**Output Characteristics**



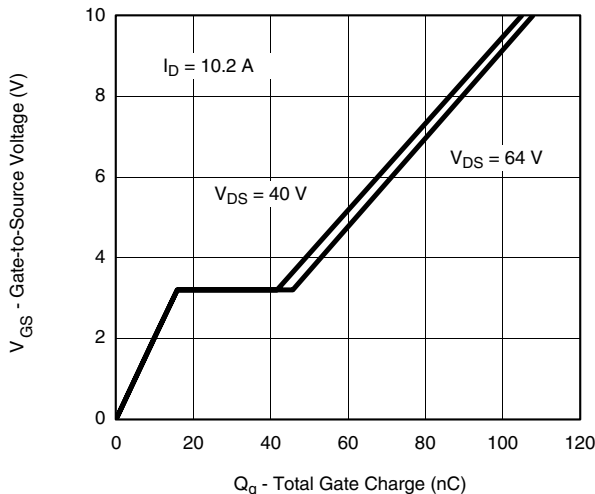
**Transfer Characteristics**



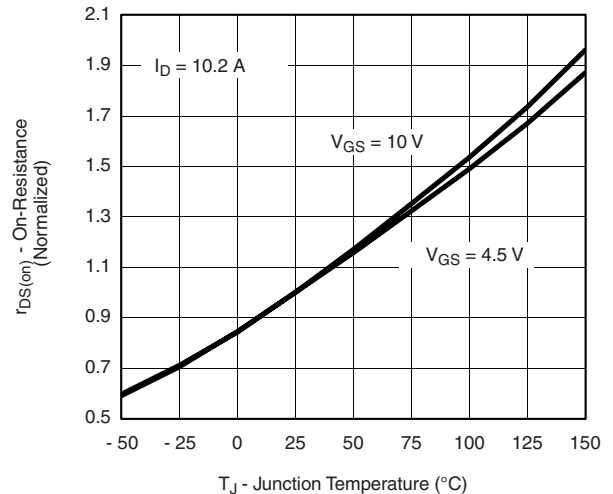
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



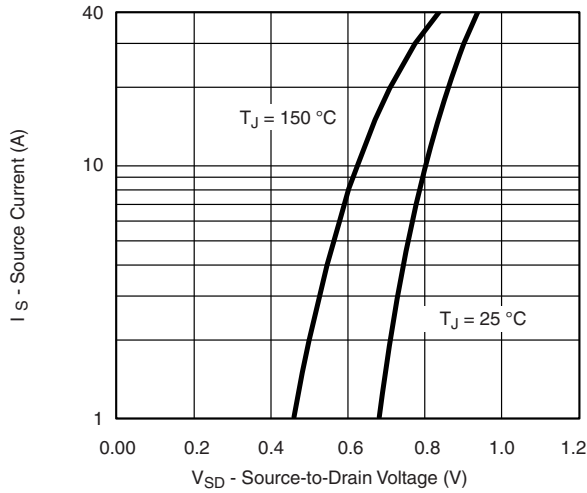
**Gate Charge**



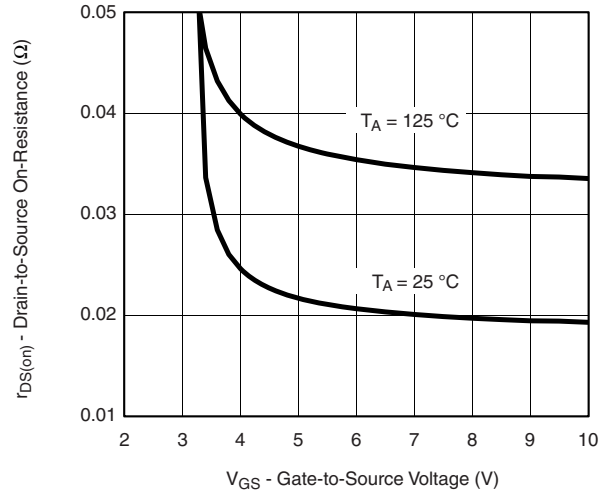
**On-Resistance vs. Junction Temperature**



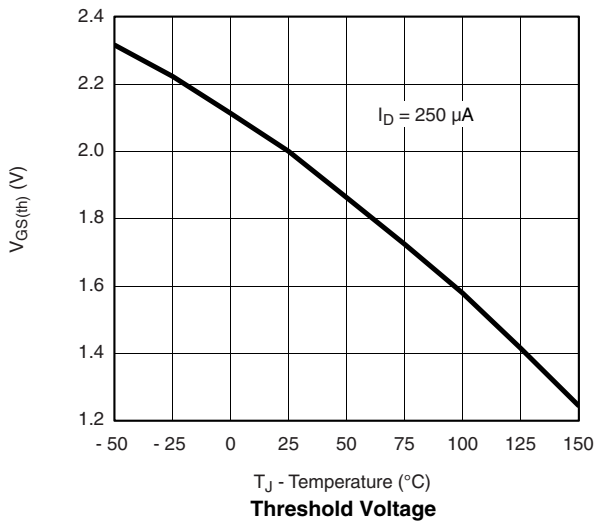
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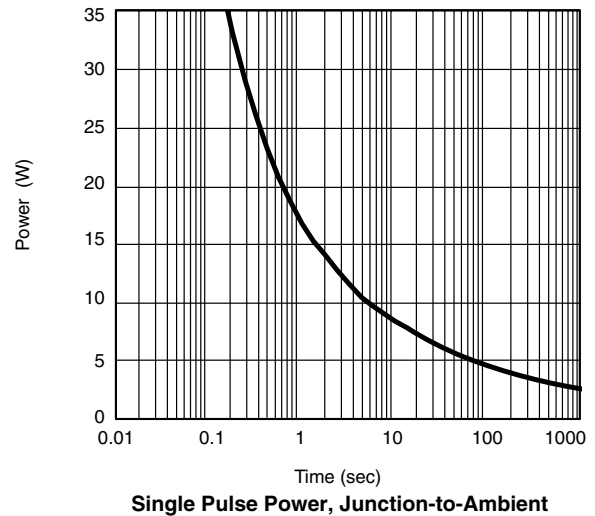
Source-Drain Diode Forward Voltage



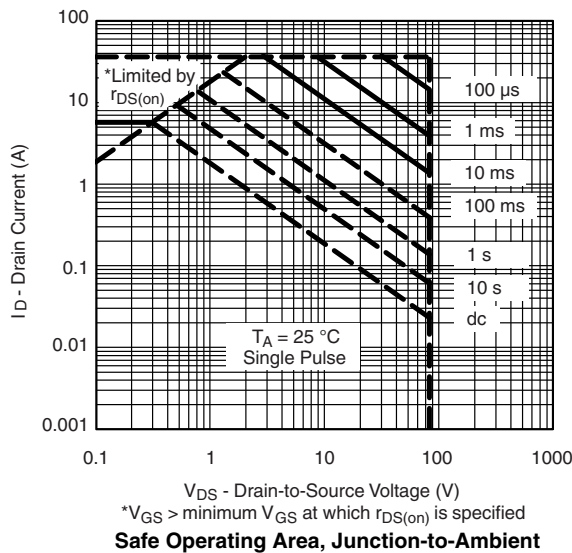
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



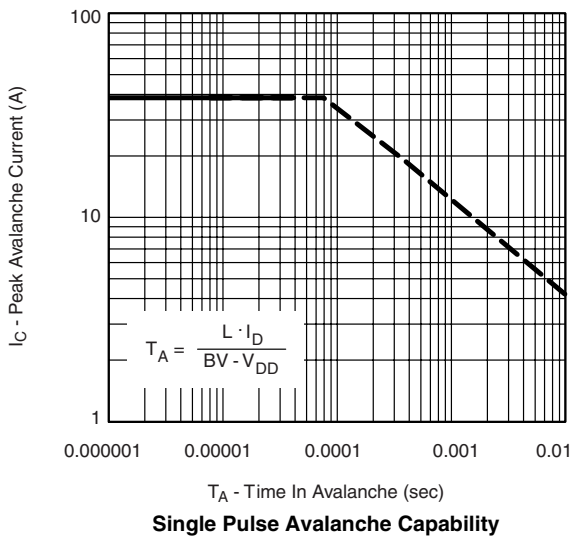
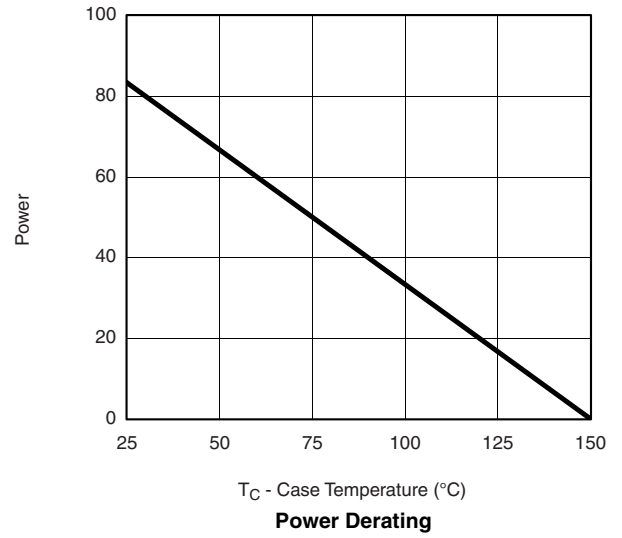
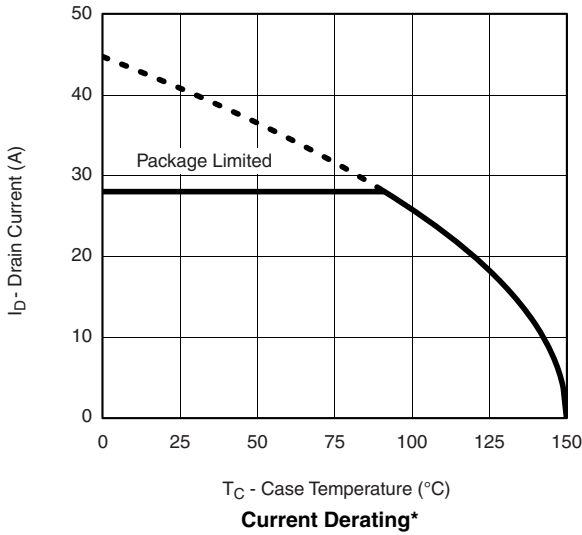
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient



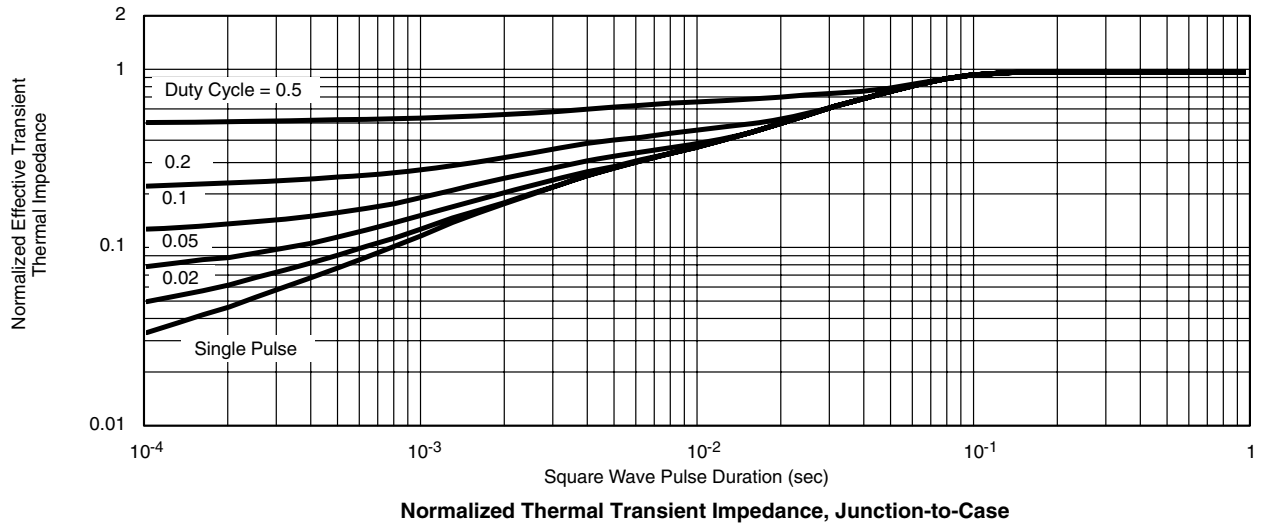
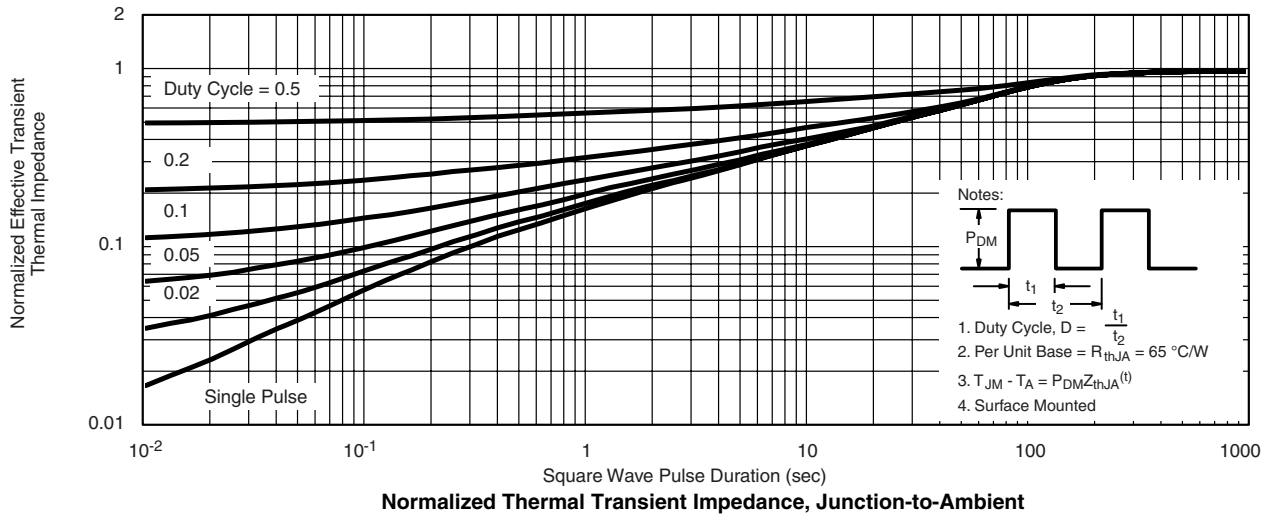
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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